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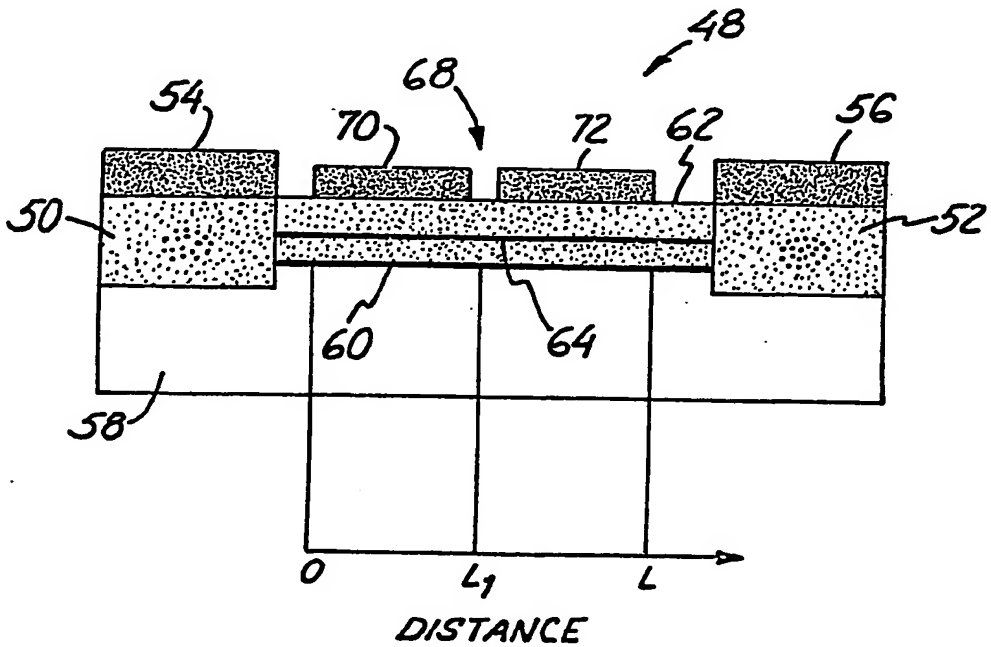

(57) Abstract

A field effect transistor (28) having a gate voltage swing in the transistor channel (40) varying as a function of position between the drain (32) and the source (30). The gate voltage swing in the transistor channel (40) may be made to vary as a function of position by making the threshold voltage a function of position. Alternatively, a split-gate device (48) may be used by applying a voltage between the gates (70, 72). In both cases, the electric field near the source (50, 30) is raised to accelerate the electrons thereby decreasing electron transit time.

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SPLIT-GATE FIELD EFFECT TRANSISTOR

BACKGROUND OF THE INVENTION

1. Field of the Invention.

The present invention relates to semiconductor devices. In particular, the invention relates to a method of increasing speed and operating frequency of field-effect transistors by the average carrier velocity in field effect transistors.

2. Description of the Prior Art.

The switching speed of field effect transistors is limited by the carrier velocity. In very short semiconductor devices electrons are expected to move ballistically, i.e. without any collisions with phonons or impurities. This may boost carrier velocity far beyond the carrier velocities in longer devices. Effective electron velocities as high as 3.25 X 10^7cm/s in a channel of a 0.08 micrometer gate-length planar-doped pseudomorphic AlGaAs/InGaAs/GaAs quantum-well High Electron Mobility Transistor (H/EMT) have been observed. This value is substantially higher than typical electron velocities in high-speed GaAs field-effect transistors (1-2 X 10^7cm/s) and somewhat larger than the peak velocity in InGaAs (approximately 2.8 X 10^7cm/s).

Nevertheless, the advantages of ballistic and/or overshoot transport are diminished in short-channel field-effect transistors compared to vertical device structures, such as a Hot Electron Transistor or a Planar-Doped Transistor. In these vertical device structures, electrons enter the active region with considerable initial velocities. Consequently, the overall transient time is decreased

thus improving the probability of ballistic transport of the electrons.

In a field effect transistor (i.e. a lateral device), on the other hand, electrons initially enter the channel with a low velocity. The electrons are gradually accelerated toward the drain due to the electric field in the field effect transistor. As numerical simulations of high-speed field effect transistors clearly indicate, the maximum electron drift velocity is reached near the drain (See, for example, A. Cappy et. al., "Comparative Potential Performance of Si, GaAs, GaInAs, InAs Submicro-meter-gate FETs", IEEE Trans. Electron Devices, Vol. ED-27, p. 2158 (1980)). The electrons move very fast in the region near the drain but relatively slow in the region near the source due to the low initial velocity of the electrons as they enter the channel. The electrons are thus more likely to experience collisions limiting their acceleration in the region near the source. The device speed is determined by the overall transit time under the gate. The device speed is heavily affected by the relatively slow electron drift velocity in the channel near the source region.

Despite a high level of interest and high speed semiconductor devices, and considerable theoretical and experimental efforts directed to the use of ballistic transport of electrons in field effect transistors and other means of increasing transistor speed, development of a high speed GaAs field effect transistor with electron velocities approaching that of vertically structured devices has yet to be achieved.

SUMMARY OF THE INVENTION

The present invention is based upon the discovery that the performance of a field effect transistor can be greatly improved if the electric field, electric potential and carrier distributions along the transistor's channel are changed in such a way that electrons are accelerated more rapidly thereby raising the average electron velocity in the channel. This may be achieved, for example, by making the device threshold voltage a function of position along the transistor channel. By choosing a more positive threshold voltage near the source of the field effect transistor (for n-channel devices) and a more negative threshold voltage for p-channel devices, we make the channel more resistive near the source, thus increasing the electric field in that region. This will lead to a more rapid acceleration of electrons near the source.

An alternative approach is to use a device with the same threshold voltage along the length of the channel but with a "split" gate. By applying a more positive gate voltage to the gate that is closer to the drain, the electric field distribution across the channel is changed in such a way that the electric field under the gate that is closer to the source becomes larger. This also causes a more rapid acceleration of electrons near the source. This differs from a conventional dual-gate field effect transistor in which the FET behaves as two field effect transistors in series. In the split-gate device, the gates are very close, so that the electric field in the channel is continuous. In practical terms, this means that the separation between the two gates should be smaller than or on

the order of the effective distance between the gate and the channel, d_{eff}. Thus, if the same gate voltage is applied to both gates, the split-gate device behaves in the same way as a single-gate device.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic diagram of a conventional planar-doped field effect transistor with a constant threshold voltage. Graphical representations of electric field and carrier velocity along the channel are shown.

Figure 2 is a schematic diagram of a planar-doped field effect transistor with lateral variation of the threshold voltage. Graphical representations of the electric field and carrier velocity along the channel are shown.

Figure 3 is a schematic diagram of a planar-doped split-gate field effect transistor.

Figure 4 is a graphical representation of the transconductance versus the gate voltage for a conventional field effect transistor and a split-gate field effect transistor.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In order to appreciate the improvement which is provided by the present invention, it is first necessary to have an understanding of electron transport in the channel of a field effect transistor. Referring to Figure 1, a conventional field effect transistor 10 is shown schematically. Field effect transistor 10 comprises a GaAs substrate 12, a doped-plane 14, a source 16, a drain 18, a source contact 20, a drain contact 22, an AlGaAs layer 24 and a gate contact 26 of length L. A channel 27 extends between source 16 and drain 18.

Figure 1 also includes graphical representations of the electric field and the electron velocity in transistor 10 along channel 27.

The threshold voltage in field effect transistor 10 is generally constant along channel 27. Electrons enter channel 27 of field effect transistor 10 from the source 16 and exit channel 24 to drain 18. The electric field along the channel is shown graphically in Figure 1 in the graph of the electric field versus distance (x). It can be seen that near source 16 of field effect transistor 10, the electric field is at its minimum value and increases exponentially to its maximum value at the edge of channel 27 near drain 18. The characteristic of this electric field causes the electrons in channel 27 to undergo relatively little acceleration in the area near source 16 of field effect transistor 10 and a substantial amount of acceleration as the electrons near drain 18. Thus, the average velocity of the electrons through channel 27 is severely limited by their relatively low velocity near source 16.

Referring now to Figure 2, a field effect transistor 28 having a threshold voltage as a function of position is shown. Field effect transistor 28 includes a source 30, a drain 32, a GaAs substrate 34, a source contact 36, a drain contact 38, a channel 40, an AlGaAs layer 42, a doped plane 43, and gate contact 44. Field effect transistor 28 also includes ion-implanted region 46. The threshold voltage of field effect transistor 28 shown in Figure 2 is a function of position along channel 40 due to ion-implanted region 46. By

choosing a more positve threshold voltage in channel 40 near source 30 the region of channel 40 near source 30 becomes more resistive, thus increasing the electric field near source 30. This is graphically shown in Figure 2 in the graph of electric field versus distance (x). Comparing the graph of electric field versus distance in Figure 2 with that of Figure 1, the electric field in channel 40 near source 30 is increased and the overall electric field is more nearly constant throughout channel 40 then in channel 27 of transistor 10.

The increased electric field near source 30 of field effect transistor 28 shown in Figure 2 leads to a more rapid acceleration of electrons near source 30. This is shown in the graph of velocity versus distance in Figure 2. Compared to Figure 1, the electrons in channel 40 experience much greater acceleration near source 30 of field effect transistor 28 in Figure 2 over similarly positioned electrons in the conventional field effect transistor 10 of Figure 1. This results in a decrease in the transit time of electrons through channel 40 of field effect transistor 28. Transit time equals the channel length divided by the average velocity ($t = L/v_{avg}$). The average velocity through the channe l is equal to the area under the curves shown in the gr aphs of velocity versus distance in Figures 1 and 2. T he average velocity may be calculated using the formula :

$$v_{avg} = \frac{\int_0^L v\,dx}{L} \qquad \text{Equation 1}$$

Where L is the length of channels 27 and 40. Thus the average velocity through channel 40 is substantially increased over that of channel 27 due to the increased area under graph of velocity in Figure 2.

Referring now to Figure 3, a split-gate field effect transistor 48 is shown. Split-gate field effect transistor 48 includes a source 50, a drain 52, a source contact 54, a drain contact 56, GaAs substrate 58, a channel 60, an AlGaAs layer 62, and a doped plane 64. Split-gate field effect transistor 48 also includes a split-gate structure 68 comprising gate contacts 70 and 72. Gate contact 70 extends generally between a left most position closest to source 50 (0) to L in the x direction shown in Figure 3. Gate contact 72 extends generally between L and L.

The split-gate field effect transistor 48 shown in Figure 3 is an alternative approach to the varying threshold voltage of the field effect transistor 28 shown in Figure 2. By applying a more positive gate voltage to gate 72 (the gate closer to drain 52) the electric field distribution across channel 60 is changed in such a way that the electric field under gate 70 (the gate closer to source 50) becomes larger. This increased electric field near source 50 causes a more rapid acceleration of electrons near source 50. The qualitive field and velocity distributions in channel 60 of split-gate field effect transistor 48 are similar to those shown graphically in Figure 2 for field effect transistor 28 having a varying threshold voltage.

The split-gate field effect transistor 48 functions differently than a conventional dual-gate field effect transistor. In a dual-gate device, the gates are separated by a relatively large distance, so that a dual-gate field effect transistor behaves as two field effect transistors in series. In the split-gate field effect transistor 48 of Figure 3, on the other hand, the gates are very close so that the electric field in the channel is continuous. If the same gate voltage is applied to both gates 70 and 72, the split-gate field effect transistor 48 behaves in the same way as a conventional field effect transistor, for example 10 in Figure 1. This means that the separation between gates 70 and 72 in split-gate field effect transistor 48 should be smaller than or on the order of the effective distance between gate 70 or 72 and channel 60 (d_{eff}).

By calculating the High Electron Mobility Transistor (HEMT) transconductance using a simple charge control model (M. Shur, GaAs Devices and Circuits, Plenum, New York (1987), for example), the advantages of a split-gate device may be illustrated. Assuming that the electron velocity in channel 60 is given by the formula:

$$v = \begin{cases} uF & F \quad F_s = v_s/\mu \\ V_s & F \quad F_s = v_s/\mu \end{cases} \qquad \text{Equation 2}$$

Where F is the electric field, μ is the effective field effect mobility and v_s is the effective electron saturation velocity. When the electric field in channel 60 is smaller than the electric

saturation field, F_s, the electric current in the channel is given by:

$$i = qn_s \mu FW \qquad \text{Equation 3}$$

Where q is the electronic charge, W is the gate width, and F is the electric field given by:

$$|F| = dV/dx \qquad \text{Equation 4}$$

V is the channel potential, x is the coordinate along the channel, and n_s is the surface carrier concentration in the channel given by:

$$n_s = \begin{cases} (c_{eff}/q)(V_{g1} - V_{t1} - V) & \text{for } 0 \text{ x } L_1 \\ (c_{eff}/q)(V_{g1} - V_{t2} - V) & \text{for } L \text{ x } L_1 \end{cases} \qquad \text{Equation 5}$$

Where V_{g1} and V_{g2} are gate voltages applied to first gate 70 and second gate 72 of split-gate field effect transistor 48 in Figure 3, V_{t1} and V_{t2} are the threshold voltages under the first and second gate 70 and 72, respectively, c_{eff} is the effective gate capacitance per unit area given by:

$$c_{eff} = \varepsilon/d_{eff} = \varepsilon/(d + \Delta d) \qquad \text{Equation 6}$$

Where d is the distance between the gate and the channel 60, Δd is the effective thickness of the two dimensional electron gas, ε is the dielectric permittivity of the semiconductor layer between the gate and channel 60.

Substituting equations 4 and 5 into equation 3 and integrating with respect to x, equations are obtained yielding the electric potential distribution in the channel V(x). The saturation current is determined from the condition that the maximum field in channel 60 is equal to F_s. Depending on the gate voltage swing and on the difference, ΔV_g, between the gate voltages applied to the two gates, the electric field may reach F_s either at $x = L_1$ or $x = L$. For example, considering the case, when $V_{t1} = V_{t2}$ but V_{g2} is greater than V_{g1} ($V_{g2} - V_{g1} = \Delta V_g$ = a constant). In this case, when V_{g1} is close to V_t the electric current is limited by the section of channel 60 under the first gate. Hence, the voltage drop, V_1, across the section of the channel increases until the saturation is reached at the end of the section of the channel under the first gate ($x = L_1$). At large gate voltage swings, the velocity saturation occurs at the drain side of the channel ($x = L$). In this case, the drain saturation current, I_s, and potential V_1 are found from the solution of the following equations, obtained by the integration described above:

$$I_s = (\mu c_{eff} W/L_1)(V_{gt1} V_1 - V_1^{\,2}/2) \qquad \text{Equation 7}$$

$$I_s(L - L_1) = \mu c_{eff} W \left\{ V_{gt2} \left[V_{gt2} - I_s/(\mu c_{eff} F_s W) - V_1 \right] - V_{gt2} - Is/(c_{eff} F_s W) \right]^2 2/_2 + V_1^{\,2}/2 \right\} \qquad \text{Equation 8}$$

Here $V_{gt2} = V_{g2} - V_{t2}$, $V_{gt1} = V_{g1} - V_{t1}$, $V_1 = V(L_1)$. Once these equations are solved, the device transconductance in the saturation regime

is calculated as $g_m = dI_s/dV_{g1}$ (taking into account that $V_{g2} = V_{g1} + \Delta V_g$).

The results of such a calculation are shown graphically in Figure 4. Line 74 was calculated using $V_g = 0$ (i.e. a conventional field effect transistor). Line 76 was calculated with $\Delta V_g = 0.1$ V (i.e a split-gate field effect transistor with a 0.1 volt difference between the two gates). As seen in Figure 4, in split-gate operation shown by line 76, the maximum transconductance is achieved at a much smaller gate voltage swing.

This simple model does not take into account an enhancement of the electron velocity due to the ballistic effects under the conditions of faster electronic acceleration in the split-gate mode of operation. This effect should increase the effective electron saturation of velocity, v_s, and hence, the maximum device transconductance.

Further analysis of this model reveals that the greatest benefit of the split-gate device occurs in materials with a relatively small electron mobility and a relatively large saturation velocity. Such materials include InP, diamond, SiC, and p-type materials.

The present invention considerably increases electron or hole transport speed in short channel field effect transistors by utilizing a lateral variation of the gate voltage swing. This is achieved by either making the threshold voltage a function of position or by using a split-gate gate field effect transistor. In both cases, a smaller gate voltage swing close to the source leads to a higher electric field in this portion of the channel

and therefore, to a more rapid increase of the electron velocity with distance. Calculations of the device transconductance using a charge-control model show that the performance in the split-gate device can be considerably improved compared to a conventional field effect transistor. Even larger improvements may be expected because of the enhancement of the ballistic transport in short channel devices caused by the faster acceleration of electrons in a split-gate field effect transistor.

In a split gate device, further improvements may be realized by using more than a single split gate pair.

WHAT IS CLAIMED IS:

1. A transistor comprising:
a drain region including a drain contact;
a source region including a source contact; and
a channel region including at least one gate contact between the drain region and the source region, having means for varying the gate voltage swing in the channel region as a function of position in a direction from the source region to the drain region.

2. The transistor of Claim 1 wherein the electric field varying means comprises ion implantation in the channel region for varying threshold voltage as a function of position in a direction from the source region to the drain region.

3. The transistor of Claim 1 wherein the means for varying the gate voltage swing comprises a plurality of gate contacts.

4. A transistor comprising:
a drain region including a drain contact;
a source region including a source contact; and;
two or more channel regions between the source and drain regions each controlled by separate gate contacts, each gate contact being closely spaced so that continuous electric field distribution is produced therebetween.

5. A method of decreasing carrier transit time in a transistor, the transistor including a drain region, a channel region and a source region, comprising the steps of:

applying an electric field to the channel region; and

varying the electric field in the channel region as a function of position in a direction from the source region to the drain region.

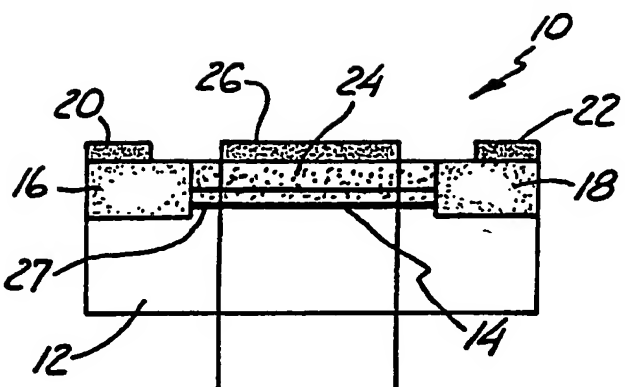
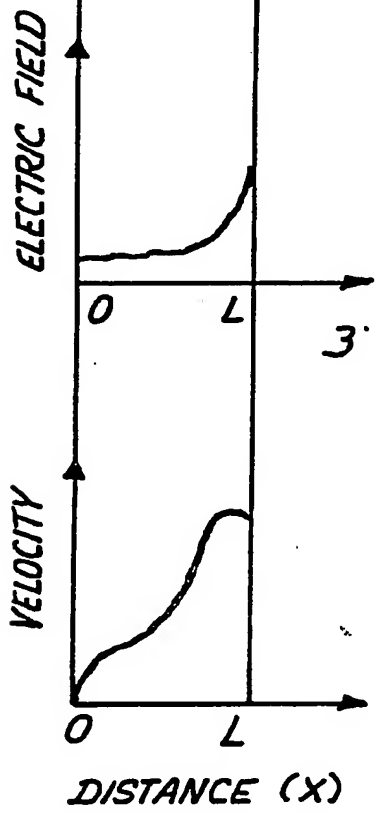
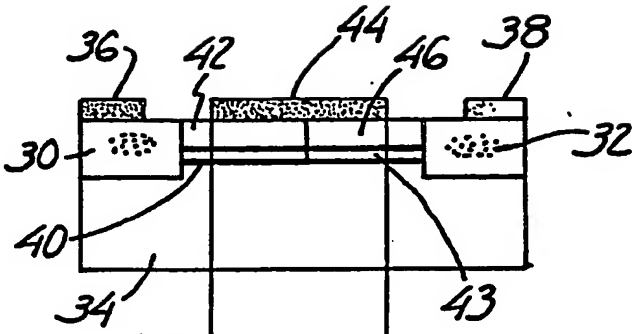


Fig.1





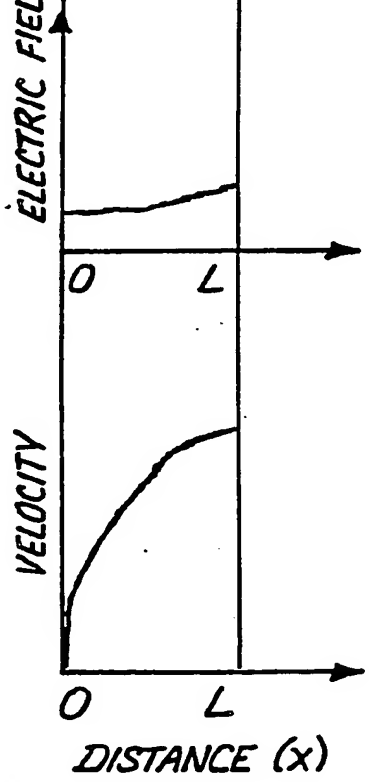


Fig.2

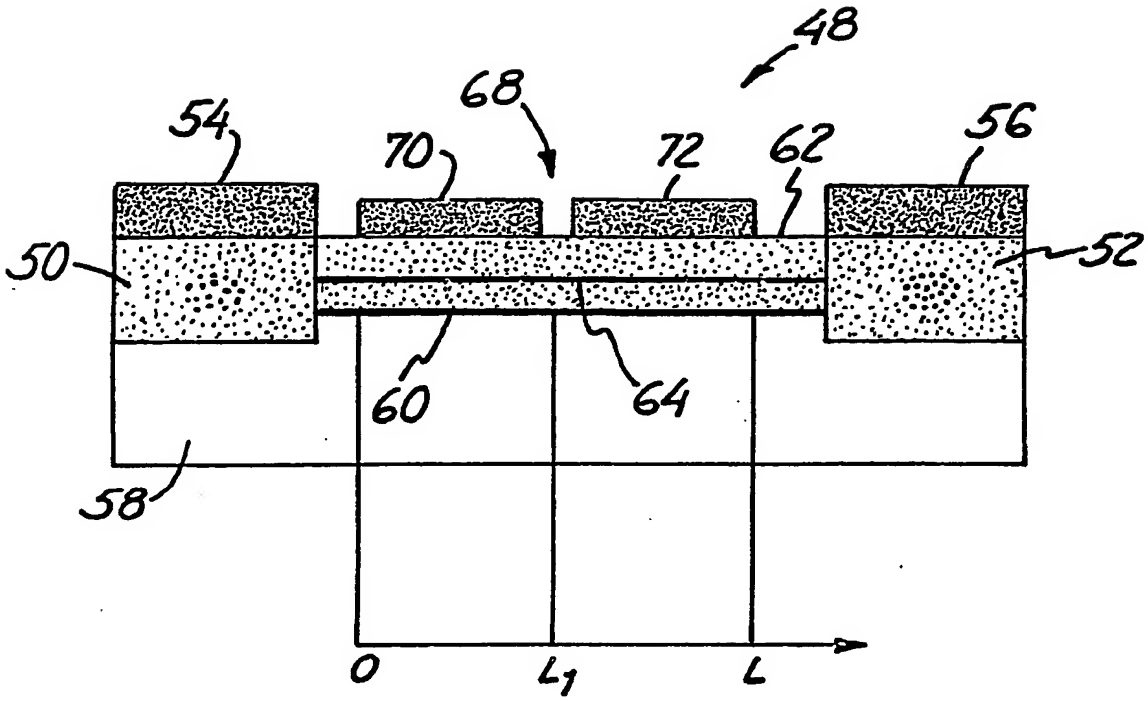


Fig.3

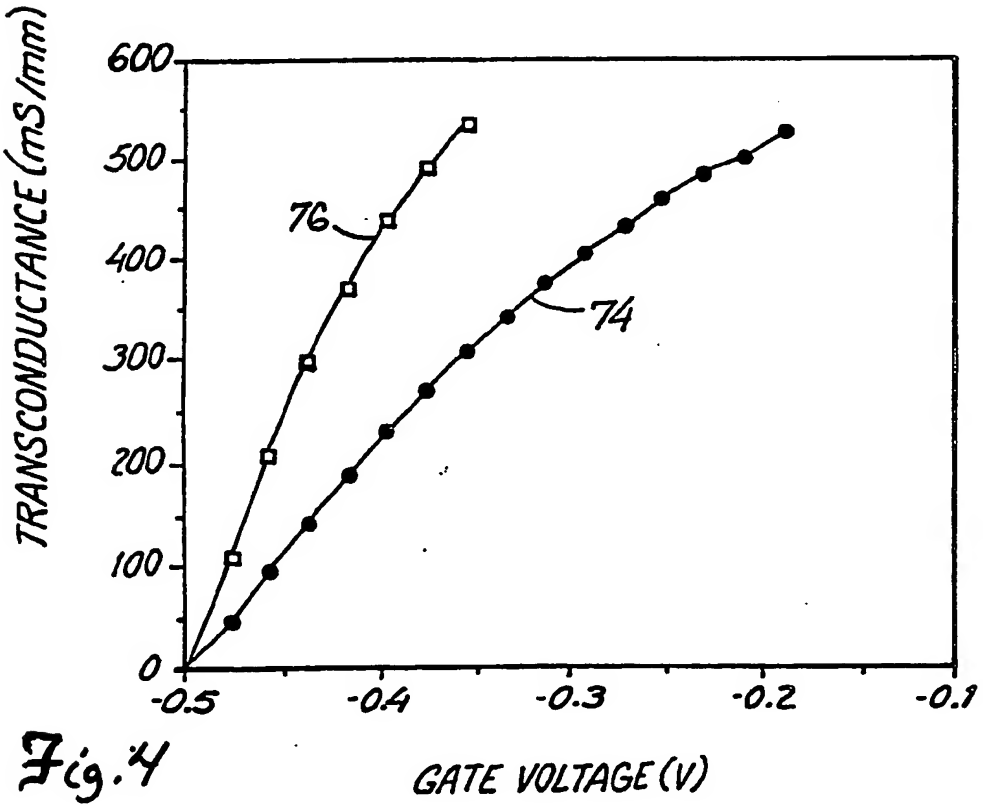


Fig.4

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 89/05861

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[5]: H 01 L 29/10, H 01 L 29/60, H 01 L 29/812

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System [8]	Classification Symbols
IPC[5]	H 01 L 29

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [9]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	1979 International Symposium on Circuits and Systems, Proceedings, 17-19 July 1979, Tokyo, Japan, IEEE, G.F. Anderson et al.: "The use of nonuniformly doped FET's in GaAs subnanosecond switching circuits: simulations", pages 784-787 see abstract; page 784, columns 1-2 --	1,5
X	Solid-State Electronics, volume 14, no. 11-D, 1971, Pergamon Press, Ltd, (Oxford, GB), T.A. Demassa et al.: "Inhomogeneous channel resistivity field effect defices", pages 1107-1112 see the abstract; figure 1 --	1,5
X	US, A, 3951708 (DEAN) 20 April 1976 see abstract; figure 10; column 1, line 36 - column 2, line 10 --	1,3-5
X	FR, A, 2550889 (THOMSON-CSF) ./.	1,3-5

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
9th May 1990	13 JUN 1990
International Searching Authority	**Signature of Authorized Officer**
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III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
	22 February 1985 see abstract; figure 1; page 7, line 18 - page 8, line 7 --	
X	IEEE Electron Device Letters, volume EDL-3, no. 8, August 1982, IEEE, (New York, US), P.C. Chao et al.: "Experimental comparisons in the electrical performance of long and ultrashort gate length GaAs MESFET's", pages 187-190 see abstract, page 188, column 2 --	1,3-5
P,X	Applied Physics Letters, volume 54, no. 2, 9 January 1989, American Institute of Physics, (New York, US), M. Shur: "Split-gate field-effect transistor", pages 162-164 see the whole article	1-5

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. US 8905861 SA 34112

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 3951708	20-04-76	None	
FR-A- 2550889	22-02-85	None	

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